ATTORNEY DOCKET NO.: 041501-5415

Application No.: 09/987,738

Page 3

IN THE CLAIMS:

Kindly amend claims 1, 3 and 7 as follows. A detailed listing of all claims is as follows.

Claim 1 (Currently Amended): A method for forming silicon quantum dots comprising the steps of:

forming a first insulating film on a semiconductor substrate;

forming a plurality of nano-crystalline silicons on the first insulating film;

forming a second insulating film on the first insulating film including the nano-crystalline silicons;

partially etching the second insulating film and the nano-crystalline silicons; and oxidizing surfaces of the etched nano-crystalline silicons.

Claim 2 (Original): The method of claim 1, wherein the nano-crystalline silicons are formed at a size of about 30nm.

Claim 3 (Currently Amended): The method of claim 1, wherein the second insulating film and the nano-crystalline silicons are etched by etching such that the second insulating film and the nano-crystalline silicons by have a height of about 10nm after the etching step.

Claim 4 (Original): The method of claim 1, wherein the nano-crystalline silicons are oxidized by about 5nm.

Claim 5 (Original): A method for fabricating a nonvolatile memory device comprising the steps of:

Page 4

forming a tunnelling insulating film on a semiconductor substrate;

forming a plurality of nano-crystalline silicons on the tunnelling insulating film;

forming a first insulating film on the tunnelling insulating film including the nano-crystalline silicons;

partially etching the first insulating film and the nano-crystalline silicons; oxidizing surfaces of the nano-crystalline silicons;

forming a second insulating film on the first insulating film including the nano-crystalline silicons;

forming a control gate on the second insulating film;

removing the second insulating film, the nano-crystalline silicons, and the tunnelling insulating film using the control gate as a mask; and

forming impurity regions in a surface of the semiconductor substrate at both sides of the control gate.

Claim 6 (Original): The method of claim 5, wherein the nano-crystalline silicons are formed at a size of about 30nm.

Claim 7 (Currently Amended): The method of claim 5, wherein the second insulating film and the nano-crystalline silicons are etched by etching such that the second insulating film and the nano-crystalline silicons by have a height of about 10nm after the etching step.

Claim 8 (Original): The method of claim 5, wherein the nano-crystalline silicons are oxidized by about 5nm.

